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Specification
(54) Title of Invention: Manufacturing Method of Thin Film Transistor
(57) Summary
[Purpose] To manufacture a thin film transistor without a high temperature thermal processing process, and to make a threshold voltage V_{th} of the thin film transistor stable and uniform.
[Means for solution] A gate electrode 41 and a gate insulating film 42 are formed on a substrate 50, and a poly-crystalline silicon thin film 10 with high impurity concentration is formed with the gate electrode 41 insulated. Then, an ion which inactivates impurity element in silicon is implanted into one portion facing the gate electrode 41 of the poly-crystalline silicon thin film 10. Accordingly, the portion becomes a channel region 1 because the carrier concentration of the portion is lowered, and the rest become source and drain regions 2. Consequently, a thin film transistor wherein the carrier concentration of the channel region 1 is controlled precisely is manufactured without a high temperature thermal processing process.

[What is claimed]
[Claim 1] A manufacturing method of a thin film transistor comprising:
a gate structure forming process for forming a gate electrode and a gate insulating film;
a depositing process for depositing a semiconductor thin film with high impurity concentration with said gate electrode insulated; and
a channel forming process for making one portion facing said gate electrode of said semiconductor thin film a channel region by ion implanting and making the rest a source region and a drain region;
wherein an ion implanted in said ion implantation inactivates an impurity element in said semiconductor thin film.

[Detailed Description of the Invention]
[0001]
[Field of the invention] The present invention relates to a manufacturing method of a thin film transistor, for example used for a switching element of an active matrix type display device, furthermore relates in detail to a manufacturing method of a thin film transistor wherein an element that a stable and uniform threshold voltage of each thin film transistor

is obtained and a multi-gradation operation is possible can be manufactured without a thermal damage on a substrate and with simple process.

[0002]

[Prior art] Conventionally, in an active matrix type display device using a material for displaying such as liquid crystal etc., a thin film transistor is used as a switching element of each pixel. The thin film transistor like this, for example, is mentioned in Japanese Patent Gazette of Laid-Open No. Sho 63-224258 etc.

[0003] The conventional manufacturing method of a thin film transistor, in outline, is manufacturing a thin film transistor shown in Figure 8 by a flow such as Figure 7. That is to say, first a gate electrode 51 of the decided shape is formed on a transparent glass substrate 50 (a). This gate electrode 51 is made of metal such as molybdenum (Mo) etc. or poly-crystalline silicon (Si). Then, a gate insulating film 52 is formed on the glass substrate 50 including this gate electrode 51 by CVD (chemical vapor phase deposition) (b), and a channel layer 53 is formed on this gate electrode 51 and the gate insulating film 52 (c). This channel layer 53 is made of amorphous silicon or poly-crystalline silicon, wherein an impurity with low concentration is doped. The threshold voltage V_{th} of operation of the thin film transistor is decided by the impurity concentration of this channel layer 53.

[0004] Next, a channel stopper layer 54 of silicon nitride (SiN_y) is formed on this channel layer 53 by plasma CVD (d). This channel stopper layer 54 becomes an etching stopper in the subsequent source and drain processing. Then, the channel layer 53 is etched into the decided shape (e), on which a source and drain layer 55 is formed to the decided shape (f), furthermore on which a source and drain electrode 56 is formed to the decided shape (g). In case that the source and drain layer 55 and the source and drain electrode 56 are etched into the decided shapes, the channel layer 53 is prevented from etching by the channel stopper layer 54. The source and drain layer 55 is made of amorphous silicon or poly-crystalline silicon, wherein an impurity with high concentration (the same impurity of pn polarity as the channel layer 53) is doped. The source and drain electrode 56 is made of metal such as aluminum (Al) etc. At last, covering a silicon nitride protective film (Figure is omitted) is performed by plasma CVD (h), consequently a thin film transistor device is accomplished.

[0005] In the thin film transistor manufactured in this way, because the channel layer 53 has high resistance for its low impurity concentration, the conductivity between the source layer 55 and the drain layer 55 is OFF under normal conditions. However, when the voltage V_g is applied to the gate electrode 51, the field effect increases the carrier concentration in the channel layer 53 so that the resistant value is lowered, consequently the conductivity between the source layer 55 and the drain layer 55 becomes ON. The gate voltage V_g causes this ON reverse is a threshold voltage V_{th}.

[0006] The manufacturing method mentioned above is that a thin film transistor is manufactured by using a transparent glass substrate 50 as a substrate for being used for a display device, and not using high temperature thermal processing, for example, ion implanting and thermal diffusion, because this glass substrate 50 is easily affected by high temperature. Accordingly, in forming the channel layer 53 (c), and forming the source and drain layer 55 (f), not a non-doped film containing no impurity is deposited, and into which an impurity is introduced and diffused subsequently, but a doped film containing an impurity from the first is deposited.

[0007]

[Problems to be solved by the Invention] However, the thin film transistor manufactured by said conventional method has problem that the threshold voltage V_{th} is variable extensively. The cause is the variable impurity concentration of the channel layer 53.

[0008] First, for making this reason clear, the relation between the impurity concentration of the channel layer 53 and the threshold voltage V_{th} is explained. A thin film transistor of this kind operates ON by which the carrier concentration in the channel layer 53 rises up to the value enough for conductivity between the source layer 55 and the drain layer 55 by the field effect of the gate voltage V_g. The gate voltage V_g necessary for this operation is the threshold voltage V_{th}. The impurity concentration of the channel layer 53 decides the original value of the carrier concentration, therefore, when the impurity concentration is varied, the threshold voltage is also varied. For example, in case that the impurity concentration is higher than the normal value, the original carrier concentration of the channel layer 53 is high, consequently the thin film transistor becomes ON by lower gate voltage V_g. That is to say, the threshold voltage V_{th} is lower than the normal value. On the other hand, in case that the impurity concentration is lower than the normal value, the threshold voltage V_{th} is higher than the normal value. Therefore, in order to obtain the precise threshold voltage V_{th}, the impurity concentration of the channel layer 53 needs to be uniform.

[0009] In said manufacturing method, this channel layer 53 is formed by depositing as a doped film containing the impurity. However, in a region with low impurity concentration, the concentration is variable extensively because it is difficult for the device to control the concentration. On that point, this method is different from ion implantation wherein the number of implanted ions can be controlled precisely. This variation of the concentration exists between thin film transistors each other on one substrate as well as between substrates. Accordingly, the threshold voltage V_{th} of each thin film transistor is variable on one substrate. Consequently, the number of gradation of display used for a display device is limited to about sixty-four, and it cannot be increased any more.

[0010] The present invention, is accomplished for resolving the problems of the conventional technology, and has the purpose to offer a manufacturing method of a thin film transistor wherein a threshold voltage V_{th} of a thin film transistor is stable and is obtained uniformly with high reproducibility without high temperature thermal processing process.

[0011]

[Means for resolving problems] A manufacturing method of a thin film transistor concerned in the present invention for accomplished said purposes is characterized by comprising:

a gate structure forming process for forming a gate electrode and a gate insulating film;

a depositing process for depositing a semiconductor thin film with high impurity concentration with said gate electrode insulated; and

a channel forming process for making one portion facing said gate electrode of said semiconductor thin film a channel region by ion implanting and making the rest a source region and a drain region;

wherein an ion implanted in said ion implantation inactivates an impurity element in said semiconductor thin film.

[0012] In this manufacturing method, after a gate electrode and a gate insulating film are

formed in a gate structure forming process, a semiconductor thin film with high impurity concentration is deposited in a depositing process. This semiconductor thin film is deposited with the impurity concentration having a suitable resistant value for a source region and a drain region of a thin film transistor. This concentration can be controlled precisely by a deposit apparatus, therefore the precision of the impurity concentration in the semiconductor thin film is high. Also, this semiconductor thin film is insulated from the gate electrode by the gate insulating film. Then, ions are implanted into one portion of the semiconductor thin film in a channel forming process. The portion into which the ions are implanted is further one portion of the portion facing the gate electrode in the semiconductor thin film. The ions implanted here inactivates the impurity element in the semiconductor thin film so as not to contribute to carrier grant. Accordingly, the portion into which this ion is implanted becomes the channel region of the thin film transistor because the carrier concentration is lowered and the resistant value is increased in spite of high impurity concentration. The portions where the ions are not implanted in the semiconductor thin film become the source region and the drain region of the thin film transistor. Besides, this ion implantation does not cause a thermal damage because a heating diffusion processing is not performed subsequently.

[0013] The thin film transistor manufactured in this way comprises the channel region which is one portion of the semiconductor thin film with high impurity concentration and into which the ions inactivating the impurity element are implanted, the source region and the drain region that the rest of said semiconductor thin film, the gate electrode facing said channel region and being wider than it, the gate insulating film insulating said gate electrode from said channel region, the source region, and the drain region.

[0014] In this thin film transistor, because the carrier concentration is lowered by making impurity element inactivate by ion implantation in the channel region, the resistant value of this region is high. Accordingly in the normal condition, the conductivity between the source region and the drain region is OFF by this channel region. Then, when a voltage V_g is applied to the gate electrode, an electric field by the voltage V_g on operates the whole channel region through the gate insulating film, and of which field effect increases the carrier concentration of the channel region, consequently the resistance of the channel region is decreased. When the voltage V_g reaches the threshold voltage V_{th}, the conductivity between the source region and the drain region becomes ON.

[0015] The gate voltage V_g necessary for reversing the thin film transistor to ON, that is to say, the threshold voltage V_{th} depends on the carrier concentration of the channel region in case that the gate voltage V_g is zero. This carrier concentration is a concentration of an active impurity element in the channel region, which is subtracted the concentration inactivated by ion implantation in the channel forming process from the impurity concentration at depositing the semiconductor thin film with high impurity concentration in the depositing process. Besides, because the impurity concentration at deposit can be controlled precisely by a deposit apparatus and the number of implanted ions can be controlled precisely in ion implantation, the concentration of the active impurity element in the channel region can be controlled precisely and the reproducibility is high. Consequently, even if a large number of thin film transistors are formed on one substrate, the uniformity of the threshold voltage V_{th} of each thin film transistor is high.

[0016] Besides, in this thin film transistor, because the channel region, the source region and the drain region are formed as one layer of the semiconductor thin film with high impurity concentration, a contact resistance between the channel region and the source and the drain regions is extremely low and a channel length can be shortened. Accordingly ON resistance is low and high-speed operation is possible.

[0017] The followings are explanations by giving preferable situations for accomplishing said purpose further satisfactorily.

[0018] [Situation 1] In a manufacturing method of a thin film transistor of claim 1, a manufacturing method of a thin film transistor wherein ion implantation in said channel forming process is performed by patterning with photoresist mask, and an electrode forming process for forming a source electrode and a drain electrode on a source region and a drain region formed on said semiconductor thin film in said channel forming process is included.

[0019] [Situation 2] In a manufacturing method of a thin film transistor of claim 1, a manufacturing method of a thin film transistor wherein an electrode forming process for forming a source electrode and a drain electrode on the portion to be a source region and a drain region of a semiconductor thin film deposited in said depositing process is included, and ion implanting is performed in said channel forming process using this source electrode and the drain electrode as pattern masks.

[0020] In manufacturing methods of these situations 1 and 2, because a source electrode and a drain electrode for a source region and a drain region are formed in an electrode forming process, an ohmic contact between the source and the drain regions and a wiring is obtained by the source electrode and the drain electrode. Especially, in the manufacturing method of situation 2, because the source electrode and the drain electrode are used as the pattern masks at ion implantation, it is not necessary to perform photolithography for ion implantation only, and the number of times of photo can be reduced.

[0021] [Situation 3] In a manufacturing method of a thin film transistor of situation 1 or situation 2, a manufacturing method of a thin film transistor wherein a stopper forming process for forming an etching stopper layer on a portion to be a channel region of a semiconductor thin film deposited in said depositing process, or on a channel region formed on said semiconductor thin film in said channel forming process is included.

[0022] In this manufacturing method, the etching stopper layer formed in the stopper forming process prevents the portion to be the channel region of the semiconductor thin film or the channel region formed on the semiconductor thin film from being etched in etching an electrode layer in an electrode forming process. For, under the condition that the electrode layer is etched, because the semiconductor thin film is also etched frequently, it is necessary to prevent it from being etched. Therefore, the timing in performing this stopper forming process can be before the electrode forming process, and also before or after forming the channel region on the semiconductor thin film in the channel forming process.

[0023] [Situation 4] In a manufacturing method of a thin film transistor of claim 1, situation 1, situation 2, or situation 3, a manufacturing method of a thin film transistor wherein a semiconductor thin film deposited in said depositing process is an amorphous silicon thin film or a poly-crystalline silicon thin film, and an ion implanted in said channel forming process is an ion of element of one or not less than two selected from a group comprising Si, F (fluorine), and Ar (argon).

[0024] In this manufacturing method, an amorphous silicon thin film or a poly-crystalline silicon thin film with high impurity concentration can be deposited controlling the impurity concentration precisely by a normal depositing apparatus. Si, F and Ar have an operation for inactivating the impurity element by which they are ionized and implanted into the amorphous silicon thin film or the poly-crystalline silicon thin film, and are suitable for forming the channel region.

[0025]

[Embodiment] An embodiment of the present invention is explained in detail referring to Figures. In a manufacturing method of a thin film transistor concerned in each embodiment explained below, a large number of thin film transistors are manufactured in a matrix shape on a transparent glass substrate for using as switching elements of a liquid crystal display device. However, for convenience' sake, only one thin film transistor is shown in Figures.

[0026] First embodiment. This embodiment corresponds to claim 1, situation 1, situation 3 concerned in situation 1, and situation 4 concerned in situation 1.

[0027] This embodiment, as shown in Figure 3, fundamentally comprises; forming a gate electrode on a glass substrate (S1), forming a gate insulating film (S2), forming a poly-crystalline silicon film as a doped film with high impurity concentration (S3), forming a channel region by implanting ions into one portion of this poly-crystalline silicon film and making the rest source and drain regions (S4), forming a channel stopper film covering this channel region (S5), removing a superfluous portion of the source and the drain regions (S6), forming the source and drain regions (S7), last of all, covering the whole with a protective film (S8). The following is a detailed explanation using Figure 1 and Figure 2.

[0028] Figure 1 (a) shows a cross sectional view of the condition to form a gate electrode 41, a gate insulating film 42 and a poly-crystalline silicon film 10 with high impurity concentration on a glass substrate 50. Among these forming processes, forming the gate electrode 41 and the gate insulating film 42 is a gate structure forming process in claim 1, and forming the poly-crystalline silicon film 10 with high impurity concentration is a depositing process in claim 1.

[0029] First, the gate electrode 41 is formed with metal such as molybdenum etc. or poly-crystalline silicon on the glass substrate 50 (S1 of Figure 3). This gate electrode 41 is formed by depositing a daubed film of metal or poly-crystalline silicon on the glass substrate 50 with sputtering or CVD, and by processing the film into the decided shape with photolithography and etching. In case of using poly-crystalline silicon, an impurity is made to contain for making sure of the conductivity.

[0030] Next, the gate insulating film 42 is formed on the glass substrate 59 including the gate electrode 41 (S2 of Figure 3). The quality of the material of the gate insulating film 42 is not limited especially if it is excellent in insulating properties, but it is general to form the film using silicon oxide (SiO_x), silicon nitride, etc. by CVD. Though the gate insulating film 42 exists on all the surface of the glass substrate 50 within range of being shown in Figure 1 (a), because it is not necessary in the portion except the thin film transistor, for example in the portion for forming a liquid crystal element etc., the unnecessary portion is removed by photolithography and etching.

[0031] Successively, the poly-crystalline silicon film 10 with high impurity concentration is

formed on the gate insulating film 42 as a daubed film by CVD (S3 of Figure 3). This poly-crystalline silicon film 10 becomes a channel region and source and drain regions in the thin film transistor, and is insulated from the gate electrode 41 by the gate insulating film 42. Then, an impurity with the decided concentration is made to contain in this poly-crystalline silicon film 10 at deposit. This impurity is an element imparting the conductivity to silicon such as phosphorus (P), boron (B), etc. The concentration of this impurity is high concentration obtaining the suitable conductivity for the source and the drain regions of the thin film transistor. Concretely, the poly-crystalline silicon film 10 with high impurity concentration is deposited by mixing impurity supplying gases such as phosphine (PH_3) and diborane (B_2H_6) as an atmosphere gas of CVD at the decided ratio. The reason for making this impurity element contain at deposit is that it cannot be made to contain by solid-phase diffusion etc. after deposit because the substrate is the glass substrate 50 being easily affected by heat. Besides, the poly-crystalline silicon film 10 is used in this case, but an amorphous silicon film can be used if it has high impurity concentration.

[0032] Figure 1 (a) shows the condition having been to S3. Subsequent Figure 1 (b) shows ion implantation in a channel forming process in claim 1.

[0033] First, in order to perform this ion implantation, a resist mask 61 is patterned by photolithography. The resist mask 61 covers the portions to be source and drain regions in the poly-crystalline silicon film 10, and has a hole in the portion to be a channel region. This hole portion is located over the gate electrode 41 and is narrower than the gate electrode. Then, the ion implantation is performed in condition that this resist mask 61 exists (S4 of Figure 3). The ion implanted here is an ion of element among Si, F, or Ar. These ions have functions not making contribute to carrier grant by inactivating the impurity element contained in the poly-crystalline silicon film 10.

[0034] When this ion is implanted, the ion penetrates into the portion where the resist mask 61 is opened in the poly-crystalline silicon film 10, and the portion becomes a channel region 1. In this channel region 1, the impurity element is inactivated by the ion implanted, and the conductivity is lowered by reducing the carrier concentration. On the other hand, because the ion is masked in the portion covered with the resist mask 61, the carrier concentration of the poly-crystalline silicon film 10 is kept high value at deposit. These portions are used for source and drain regions. After the ion implantation, the resist mask 61 is removed. Besides, because the thermal diffusion is not performed after this ion implantation, the glass substrate 50 is not damaged thermally.

[0035] Next, as shown in Figure 1 (c), a channel stopper 43 of silicon nitride is formed on the poly-crystalline silicon film 10 by CVD (S5 of Figure 3). The channel stopper 43 is an etching stopper for preventing the channel region 1 from being etched in an etching processing of the source and drain electrodes mentioned later, and formed so as to cover the channel region 1 and to jut out a little into the outside. Forming this channel stopper 43 is a stopper forming process in situation 3.

[0036] Successively, as shown in Figure 2 (a), the unnecessary portion of the poly-crystalline silicon film 10 is removed by photolithography and etching. Consequently, source and drain regions 2 are processed (S6 of Figure 3). Besides, forming the channel stopper 43 of Figure 1 (c) and processing these source and drain regions 2 can be exchanged in order.

[0037] Next, as shown in Figure 2 (b), source and drain electrodes 44 are formed on the

source and drain region 2 with metal such as aluminum etc. (S7 of Figure 3). Forming these source and drain electrodes 44 is performed by forming a daubed film of the metal by sputtering or CVD and processing by photolithography and etching. In this etching process, because the poly-crystalline silicon film 10 is also etched under the condition of etching the source and drain electrodes 44, it is possible that the channel region 1 is damaged so that it is necessary to take measures to prevent it. In this case, the channel stopper 43 performs preventing function for protecting the channel region 1. The source and drain electrodes 44 formed in this way cover the upper side of the source and drain regions, and ohmic contact between them can be obtained. Forming the source and drain electrodes 44 is an electrode forming process in situation 1.

[0038] Then, after forming the necessary wiring, as shown in Figure 2 (c), a protective film 45 of silicon nitride or silicon oxide is formed by CVD and covers the whole (S8 of Figure 3), consequently a thin film transistor device is accomplished.

[0039] The thin film transistor manufactured in this way comprises: the channel region 1 which is one portion of the poly-crystalline silicon film 10 with high impurity concentration and wherein an impurity element is inactivated by performing ion implantation of element among Si, F, and Ar; the source and drain regions 2 that the rest of the poly-crystalline silicon film 10; the gate electrode 41 facing the channel region 1 and provided wider than the channel region 1; the gate insulating film 42 insulating the channel region 1 and the source and drain regions 2 from the gate electrode 41; and the source and drain electrodes 44 coming into ohmic contact with the source and drain regions 2. A large number of the thin film transistors of this kind are provided in matrix shape on the glass substrate 50, and operate as switching elements of the liquid crystal display device.

[0040] The thin film transistor like this has high resistant value of the channel region 1. For, in this region, the carrier concentration is lowered because the impurity element is inactivated by ion implantation. Accordingly in the normal condition, when the voltage is applied between the source and drain regions 2 with the source and drain electrodes 44, these are not conducted each other. However, when the voltage is applied to the gate electrode 41, an electric field by the voltage V_g affects the whole of the channel region 1 through the gate insulating film 42, of which field effect increases the carrier concentration of the channel region 1 and the resistance is decreased. Then, when the gate voltage V_g reaches the threshold voltage V_{th}, an electricity is conducted between the source and drain regions 2. That is to say, the thin film transistor is reversed to ON.

[0041] The gate voltage V_g necessary for ON reverse of the thin film transistor, that is to say, the threshold voltage V_{th} depends on the carrier concentration of the channel region 1 in case that the gate voltage V_g is zero (hereinafter referred to as an original carrier concentration). The original carrier concentration is a concentration of active impurity element in the channel region 1, which is subtracted the concentration inactivated by ion implantation (S4 of Figure 3) from the impurity concentration at depositing the poly-crystalline silicon film 10 with high impurity concentration (S3 of Figure 3). Because the poly-crystalline silicon film 10 is deposited with high impurity concentration here, the concentration can be controlled precisely at CVD apparatus, and the precision of the impurity concentration of the poly-crystalline silicon film 10 is high. Then, the number of ions implanted is controlled precisely in ion implantation. Therefore, the original carrier concentration in the channel

region 1 is precise. Accordingly, the uniformity of the threshold voltage V_{th} of each thin film transistor formed on one substrate is high.

[0042] This means that the multi-gradation operation of the liquid crystal display device is possible. According to this thin film transistor, the number of gradation of display operation on the liquid crystal display device can be not less than 128.

[0043] Also, in this thin film transistor, because the channel region 1 and the source and drain regions 2 are deposited as the poly-crystalline silicon film 10 with higher impurity concentration, and the channel region 1 is distinguished from the source and drain regions 2 by ion implantation, the contact resistance between the channel region 1 and the source and drain regions 2 can be almost left out of consideration. Also, the channel length can be shortened. Accordingly the resistance at ON reverse is small and high-speed operation is possible. Especially, in case of using n-type phosphorus etc. as the impurity element of the poly-crystalline silicon film, because the mobility of electrons is higher than that of holes, furthermore high-speed operation is possible.

[0044] Besides, forming the channel region1 and the source and drain regions 2 as one layer of the poly-crystalline silicon film 10 in this thin film transistor reduces one time of photolithography and the number of photo mask, therefore, it does not make the manufacturing process complicated and is profitable in manufacturing cost.

[0045] Also, because a high temperature thermal processing such as thermal diffusion etc. is not used, a thin film transistor can be formed on a substrate without causing thermal damage. Consequently, this method is suitable for forming a thin film transistor as a switching element of a liquid crystal display device on a glass substrate affected easily by high temperature.

[0046] According to the first embodiment explained above in detail; because the poly-crystalline silicon film 10 with high impurity concentration is deposited, of which one portion is made to be the channel region 1 by performing inactivation of impurity element with ion implantation and the rest is used as the source and drain regions 2, a large number of thin film transistors can be manufactured on the glass substrate 50 without heating up to high temperature excessively so as to make threshold voltage V_{th} uniform in simple manufacturing process. Besides, in the thin film transistor manufactured in this way, ON resistance is low and high-speed operation is possible. Consequently, multi-gradation operation and high-speed operation of the liquid crystal display device are possible.

[0047] The second embodiment. This embodiment corresponds to claim 1, situation 2, situation 3 concerned in situation 2, and situation 4 concerned in situation 2.

[0048] This embodiment, as shown in Figure 6, fundamentally comprises; forming a gate electrode on a glass substrate (S11), forming a gate insulating film (S12), forming a poly-crystalline silicon film as a doped film with high impurity concentration (S13), forming a channel stopper film covering a portion to be a channel region in the poly-crystalline silicon film (S14), removing a superfluous portion (S15), forming source and drain electrodes (S16), forming a channel region on one portion of the poly-crystalline silicon film by implanting ions and making the rest source and drain regions (S17), last of all, covering the whole with a protective film (S18). The following is a detailed explanation using Figure 4 and Figure 5, quoting the previous description common to the first embodiment, and emphasizing a point of difference.

[0049] Forming the gate electrode 41 on the glass substrate 50 (S11 of Figure 6), forming the gate insulating film 42 (S12 of Figure 6), and forming the poly-crystalline silicon film 10 (an amorphous silicon film is possible) with high impurity concentration (S13 of Figure 6) are the same as those of the first embodiment (S1 to S3 of Figure 3). Figure 4 (a) shows the condition having been to S13 and the same structure of Figure 1 (a).

[0050] Next, as shown in Figure 4 (b), a channel stopper 43 of silicon nitride is formed on the poly-crystalline silicon film 10 by CVD (S14 of Figure 6). The channel stopper 43 is an etching stopper for preventing the portion to be a channel region in the poly-crystalline silicon film 10 by ion implantation mentioned later from being etched in an etching process of the source and drain electrodes mentioned later, is formed so as to cover the portion and to jut out a little into the outside. This channel stopper 43 and its formation is the same as the explained matter by S5 of Figure 3 of the first embodiment (Figure 1 (c)). However, in this embodiment, a total film thickness of the channel stopper 43 and the poly-crystalline silicon film 10 needs to be thinner than a film thickness of the gate insulating film 42. For, ions are prevented from penetrating into the glass substrate 50 in ion implantation mentioned later.

[0051] Successively, as shown in Figure 4 (c), an unnecessary portion of the poly-crystalline silicon film 10 is removed by photolithography and etching (S15 of Figure 6). By this etching, only the portions to be the channel region and the source and drain regions of the thin film transistor in the poly-crystalline silicon film 10 remain. This etching corresponds to Figure 2 (a) and S6 of Figure 3 in the first embodiment. Besides, forming the channel stopper 43 of Figure 4 (b) and this etching process can be exchange in order.

[0052] Then, as shown in Figure 5 (a), the source and drain electrodes 44 are formed with metal of aluminum etc. on the portions to be the source and drain regions in the poly-crystalline silicon film 10 (S16 of Figure 6). Forming the source and drain electrodes 44 is performed by forming a daubed film of metal by sputtering or CVD, on which a resist mask 62 is formed by photolithography, and processing the daubed film by etching. In this etching process, because the poly-crystalline silicon film 10 is etched under the condition of etching the source and drain electrodes 44, it is possible that the portion to be the channel region is damaged and it is necessary to take measures to prevent the film from being etched. In this case, the channel stopper 43 performs preventing function for protection of the film. The source and drain electrodes 44 formed in this way cover the upper side of the portions to be the source and drain regions, and ohmic contact between them can be obtained. Forming the source and drain electrodes 44 is an electrode forming process in situation 2, and corresponds to Figure 2 (b) and S7 of Figure 3 in the first embodiment.

[0053] Next, the channel region 1 is formed by ion implantation (S17 of Figure 6 and Figure 5 (b)). This ion implantation corresponds to Figure 1 (b) and S4 of Figure 3 in the first embodiment, and is a channel forming process in situation 2. Therefore the implanted ion is the ion of element among Si, F and Ar. In this case, because the resist mask 62 in itself made in the previous forming process for the source and drain electrodes 44 masks ions by functioning as a stopper against ions, ions are not implanted into the portion to be the source and drain regions and implanted into only the portion to be the channel region in the poly-crystalline silicon film 10. In the portion, the impurity element is inactivated by the implanted ion, and the conductivity is lowered by which the carrier concentration is reduced, consequently this portion becomes the channel region 1. On the other hand, because the ion

is masked in the portion covered with the resist mask 62 and the source and drain electrodes 44, the carrier concentration is kept high value at deposit. These portions are used for the source and drain regions 2. Besides, because thermal diffusion is not performed after this ion implantation, the glass substrate 50 is not damaged thermally.

[0054] At this time, the acceleration energy of the implanted ion is a low energy that ions is not passed through the gate insulating film 42 in a region outside the resist mask 62 and the source and drain electrodes 44 in Figure 5 (b). Because the glass substrate 50 in this portion is covered with only the gate insulating film 42, in case of implanting with too high energy, ions penetrate into the glass substrate 50 through the gate insulating film 42, and cause unfavorable phenomena as a display device such as cloud of the glass etc. On the other hand, energy to some extent is necessary as the implanted ions distribute over the whole thickness of the poly-crystalline silicon film 10. When the acceleration energy is too low, the portion where the carrier concentration is high remains in the portion a little to the gate insulating film 42 in a thickness of the poly-crystalline silicon film 10, and obstruction in the function as a thin film transistor is caused. In this case, as above-mentioned, because a total film thickness of the channel stopper 43 and the poly-crystalline silicon film 10 is thinner than a film thickness of the gate insulating film 42, the acceleration energy wherein ions do not penetrate into the glass substrate 50 and distribute over the whole thickness of the poly-crystalline silicon film 10 can be chosen.

[0055] Besides, the ion implantation is performed leaving the resist mask 62 as it is in Figure 5 (b), but the ion implantation can be performed after removing the resist mask 62. For, a self-alignment function of the source and drain electrodes 44 having the same pattern as the resist mask 62 prevents ion implantation into the portion except the portion to be the channel region.

[0056] Then, after forming a necessary wiring, a protective film 45 of silicon nitride or silicon oxide is formed by CVD as shown in Figure 5 (c), and covers the whole (S18 of Figure 6), consequently a thin film transistor device is accomplished.

[0057] The thin film transistor manufactured in this way has the same constitution as that of the first embodiment. That is to say, it comprises: the channel region 1 which is one portion of the poly-crystalline silicon film 10 with high impurity concentration and wherein the impurity element is inactivated by implanting ion of element among Si, F, and Ar; the source and drain regions 2 that the rest of the poly-crystalline silicon film 10; the gate electrode 41 facing the channel region 1 and provided wider than the channel region 1; the gate insulating film 42 insulating the channel region 1 and the source and drain regions 2 from the gate electrode 41; and the source and drain electrodes 44 obtaining ohmic contact with the source and drain regions 2. A large number of the thin film transistors of like this are provided in matrix shape on the glass substrate 50, and operate as switching elements of the liquid crystal display device.

[0058] Therefore, in the same way as the first embodiment, the thin film transistor of the second one has the characteristics that the threshold voltage V_{th} of each thin film transistor has high uniformity, accordingly a multi-gradation operation of the liquid crystal display device is possible. Besides, because the contact resistance between the channel region 1 and the source and drain regions 2 can be almost left out of consideration and the channel length can be shortened, the thin film transistor of the second embodiment is also the same as the

first one on the point that ON resistance is small and high-speed operation is possible. Furthermore, needless to say, the channel region 1 and the source and drain regions 2 are deposited as one layer of the poly-crystalline silicon film 10, and photolithography only for the ion implantation using the resist mask 62 for the source and drain electrodes 44 processing or the source and drain electrodes 44 themselves as pattern masks is not performed, consequently, the manufacturing processes are cut sharply. Besides, because high temperature thermal processing is not performed, a thin film transistor can be formed on a glass substrate easily affected by heat, and can be used for a switching element of a liquid crystal display device.

[0059] According to the second embodiment explained in detail above, the poly-crystalline silicon film 10 with high impurity concentration is deposited, the source and drain electrodes 44 are formed on the portions to be the source and drain regions 2 in the poly-crystalline silicon film 10, the channel region 1 is formed by which inactivation of impurity element is performed by ion implantation on the portion not covered with the source and drain electrodes 44 in the poly-crystalline silicon film 10, and the rest is used for the source and drain regions 2, consequently, a large number of thin film transistors can be manufactured on a glass substrate 50 without heating up to high temperature excessively so as to unify their threshold voltages V_{th}, with simple manufacturing processes. In the thin film transistor manufactured in this way, ON resistance is low and high-speed operation is possible. Accordingly, the multi-gradation operation and high-speed operation are possible.

[0060] Explanations based the first and the second embodiments are performed above, however, the present invention is not limited to said each embodiment in any way, needless to say, various designs can be changed within range of the gist of the present invention. For example, the concrete ingredient of various thin films such as an insulating film, a metal film, etc. shown in said each embodiment can be exchanged to other one having the same function.

[0061] Also, an example for forming a thin film transistor on a glass substrate for using as a switching element of a liquid crystal display device is shown in said each embodiment, besides, the present invention can be applied in case that a thin film transistor is formed on an object easily affected by high temperature thermal processing. For example, it is thought that it can be applied to forming a transistor after the second layer of the three-dimensional integrated circuit. For, an aluminum wiring etc. for a transistor of the first layer manufactured previously is easily affected by high temperature thermal processing.

[0062]

[Effect] According to a manufacturing method of a thin film transistor concerned in the present invention, a semiconductor thin film with high impurity concentration is deposited, inactivation of impurity element is performed by ion implantation on one portion of the semiconductor film to be a channel region, and the rest become source region and drain regions, consequently a stable and uniform threshold voltage V_{th} of a thin film transistor manufactured is obtained. Besides, because high temperature thermal processing process is not used, the thin film transistor of this kind can be formed on a substrate easily affected by high temperature.

[A brief explanation of Figures]

[Figure 1] An explanatory view of a manufacturing method of a thin film transistor

concerned in the first embodiment.

[Figure 2] An explanatory view of a manufacturing method of a thin film transistor concerned in the first embodiment.

[Figure 3] A figure showing a flow of a manufacturing method of a thin film transistor shown in Figures 1 and 2.

[Figure 4] An explanatory view of a manufacturing method of a thin film transistor concerned in the second embodiment.

[Figure 5] An explanatory view of a manufacturing method of a thin film transistor concerned in the second embodiment.

[Figure 6] A figure showing a flow of a manufacturing method of a thin film transistor shown in Figures 4 and 5.

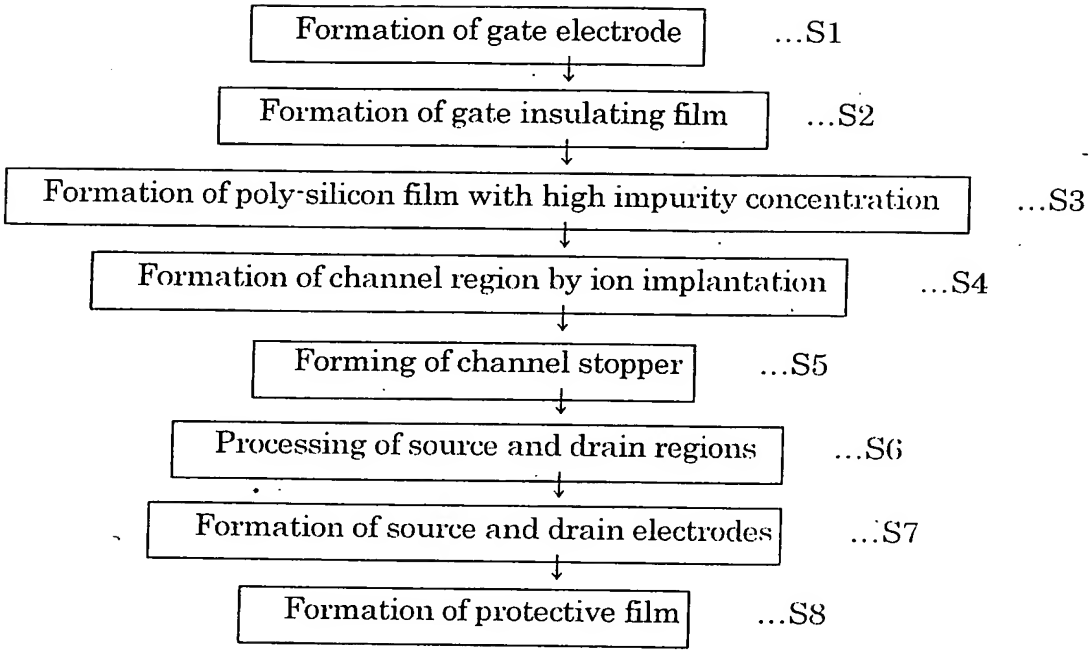
[Figure 7] A figure showing a flow of the conventional manufacturing method of a thin film transistor.

[Figure 8] An explanatory view of the conventional manufacturing method of a thin film transistor.

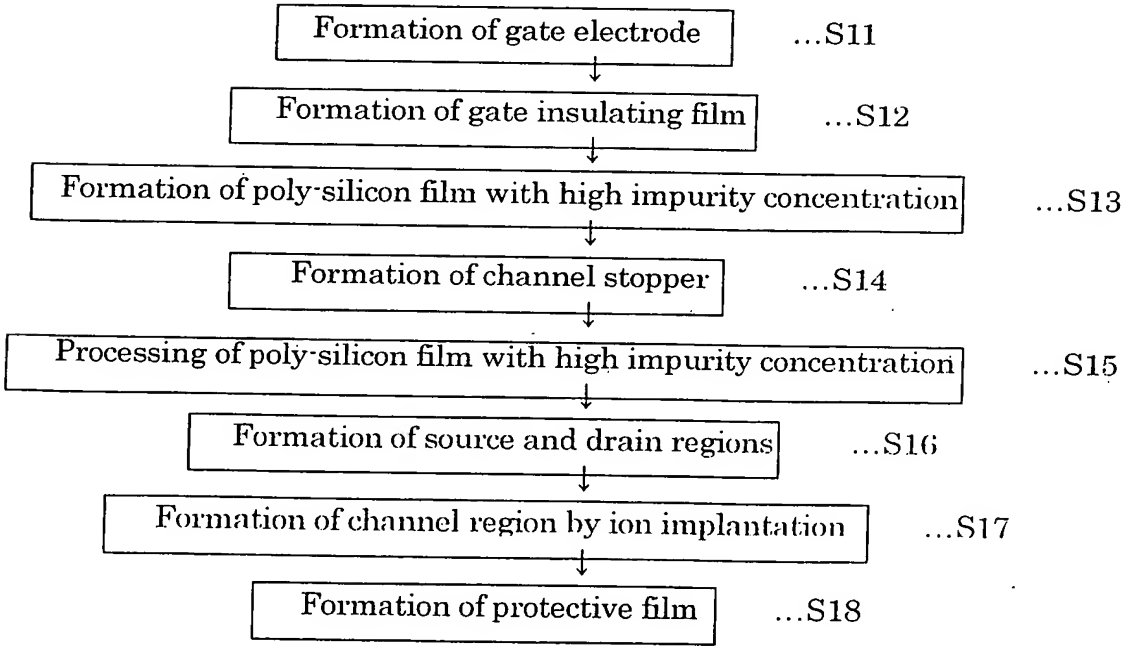
[Explanations of marks]

1 channel region
2 source and drain regions
10 poly-crystalline silicon film
41 gate electrode
42 gate insulating film

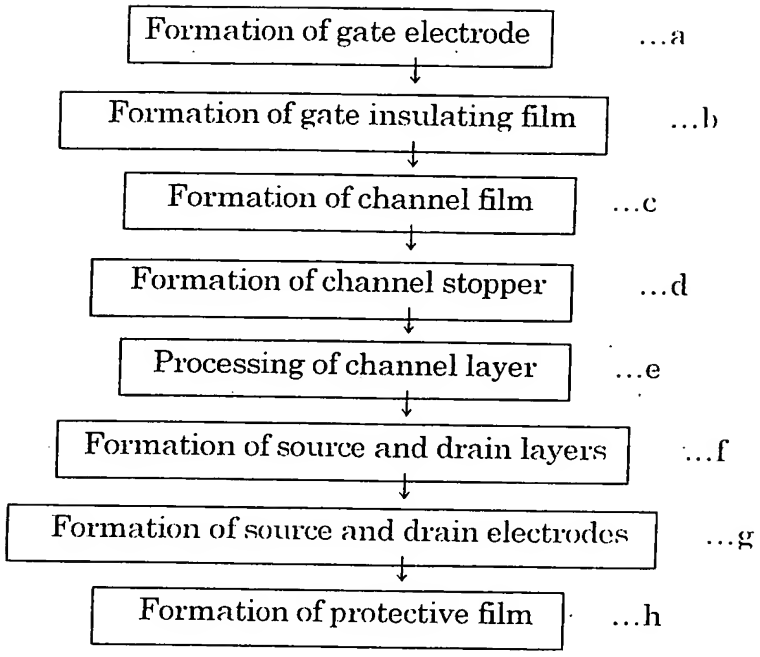
[Figure 3]



[Figure 6]



[Figure 7]


Formation of gate electrode
...a
Formation of gate insulating film
...b
Formation of channel film
...c
Formation of channel stopper
...d
Processing of channel layer
...e
Formation of source and drain layers
...f
Formation of source and drain electrodes
...g
Formation of protective film
...h